F1031

CU INTERCONNECTS WITH COMPOSITE BARRIER LAYERS FOR WAFER-TO-WAFER UNIFORMITY

TECHNICAL FIELD

[01] The present invention relates to copper (Cu) and/or Cu alloy metallization in semiconductor devices, and to a method for manufacturing semiconductor devices, and to a method for manufacturing semiconductor devices with reliable, low resistance Cu or Cu alloy interconnects. The present invention is particularly applicable to manufacturing high speed integrated circuits having submicron design features and high conductivity interconnect structures.

BACKGROUND ART

[02] The escalating requirements for high density and performance associated with ultra large scale integration semiconductor wiring require responsive changes in interconnection technology. Such escalating requirements have been found difficult to satisfy in terms of providing reliable low RxC (resistance x capacitance) interconnect patterns with higher electromigration resistance.

[03] Conventional semiconductor devices comprise a semiconductor substrate, typically doped monocrystalline silicon, and a plurality of sequentially formed interlayer dielectrics and conductive patterns. An integrated circuit is formed containing a plurality of conductive patterns comprising conductive lines separated by interwiring spacings, and a plurality of interconnect lines, such as bus lines, bit lines, word lines and logic interconnect lines. Typically, the conductive patterns on different layers, i.e., upper and lower layers, are electrically connected by a conductive plug filling a via hole, while a conductive plug filling a contact hole establishes electrical contact with an active region on a semiconductor substrate, such as a source/drain region. Conductive lines are formed in trenches which typically extend substantially horizontal with respect to the semiconductor substrate. Semiconductor "chips" comprising five or more levels of metallization are becoming more prevalent as device geometry's shrink to submicron levels.

[04] A conductive plug filling a via hole is typically formed by depositing an interlayer dielectric on a conductive layer comprising at least one conductive pattern, forming an opening through the interlayer dielectric by conventional photolithographic and etching techniques, and

filling the opening with a conductive material, such as tungsten (W). Excess conductive material on the surface of the interlayer dielectric is typically removed by chemical mechanical polishing (CMP). One such method is known as damascene and basically involves forming an opening in the interlayer dielectric and filling the opening with a metal. Dual damascene techniques involve forming an opening comprising a lower contact or via hole section in communication with an upper trench section, which opening is filled with a conductive material, typically a metal, to simultaneously form a conductive plug in electrical contact with a conductive line.

[05] High performance microprocessor applications require rapid speed of semiconductor circuitry. The control speed of semiconductor circuitry varies inversely with the resistance and capacitance of the interconnection pattern. As integrated circuits become more complex and feature sizes and spacings become smaller, the integrated circuit speed becomes less dependent upon the transistor itself and more dependent upon the interconnection pattern. Miniaturization demands long interconnects having small contacts and small cross-sections. As the length of metal interconnects increases and cross-sectional areas and distances between interconnects decrease, the RxC delay caused by the interconnect wiring increases. If the interconnection node is routed over a considerable distance, e.g., hundreds of microns or more as in submicron technologies, the interconnection capacitance limits the circuit node capacitance loading and, hence, the circuit speed. As design rules are reduced to about 0.15 micron and below, e.g., about 0.12 micron and below, the rejection rate due to integrated circuit speed delays significantly reduces production throughput and increases manufacturing costs. Moreover, as line widths decrease electrical conductivity and electromigration resistance become increasingly important.

[06] Cu and Cu alloys have received considerable attention as a candidate for replacing Al in interconnect metallizations. Cu is relatively inexpensive, easy to process, and has a lower resistively than Al. In addition, Cu has improved electrical properties vis-à-vis W, making Cu a desirable metal for use as a conductive plug as well as conductive wiring.

[07] An approach to forming Cu plugs and wiring comprises the use of damascene structures employing CMP. However, due to Cu diffusion through inter dielectric layer materials, such as silicon dioxide, Cu interconnect structures must be encapsulated by a diffusion barrier layer. Typical diffusion barrier metals include tantalum (Ta), tantalum nitride (TaN), titanium nitride (TiN), titanium (Ti), titanium-tungsten (TiW), tungsten (W), tungsten nitride (WN), Ti-TiN, titanium silicon nitride (TiSiN), tungsten silicon nitride (WSiN), tantalum silicon nitride (TaSiN) and silicon nitride for encapsulating Cu. The use of such barrier materials to encapsulate Cu is not limited to the interface between Cu and the dielectric interlayer, but includes interfaces with other metals as well.

[08] In implementing Cu metallization, particularly in damascene techniques wherein an opening is formed in a dielectric layer, particularly a dielectric layer having a low dielectric constant, e.g., a dielectric constant less than about 3.9, various reliability, electromigration and resistance issues are generated. Reliability issues stem, in part, from the use of Ta or TaN, the barrier layers of choice in Cu metallization. Ta has been found to lack adequate adhesion to various interlayer dielectric materials, particularly, interlayer dielectric materials having a low dielectric constant, e.g., a dielectric constant (k) less than about 3.9. TaN has been found to lack adequate adhesion to Cu and Cu alloys filling a damascene opening. Moreover, Ta and TaN are typically deposited by physical vapor deposition (PVD) techniques, such as ionized (I) PVD. The resulting layer of Ta is typically β-phase Ta or β-Ta which exhibits a relatively high resistivity, e.g., about 170 to about 230 μohm-cm. TaN is typically deposited with a nitrogen (N_2) content of about 30 to about 55 at.%, and exhibits a resistivity in excess of 200 μohm-cm.

[09] The adhesion problems adversely impact electromigration resistance and device reliability, while the high resistivity of TaN and β-Ta manifestly adversely impact circuit speed. Accordingly, there exists a need for reliable, low resistance Cu and Cu alloy interconnects, particularly interconnects formed in low dielectric constant materials, and for enabling methodology.

DISCLOSURE OF THE INVENTION

[10] An advantage of the present invention is a semiconductor device having reliable, low resistance Cu or Cu alloy interconnects exhibiting improved electromigration resistance and wafer-to-wafer uniformity.

[11] Additional advantages and other features of the present invention will be set forth in the description which follows and, in part, will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from the practice of the present invention. The advantages of the present invention may be realized and obtained as particularly pointed out in the appended claims.

[12] According to the present invention, the foregoing and other advantages are achieved in part by a semiconductor device having a copper (Cu) or Cu alloy interconnect comprising: an opening formed in a dielectric layer; a tantalum nitride (TaN) layer lining the opening; a graded tantalum nitride layer on the TaN layer; a continuous layer of α-tantalum (α-Ta) on the graded tantalum nitride layer; and Cu or a Cu alloy filling the opening, wherein the ratio of the thickness of the combined α-Ta and graded tantalum nitride layers to the thickness of the TaN layer is about 2:1 to about 6:1.

[13] Embodiments of the present invention include forming the composite barrier layer such that the ratio of the thickness of the combined α-Ta and graded tantalum nitride layers to the thickness of the TaN layer is about 2.5 to about 3.5, depositing the TaN layer at a thickness no greater than about 100 Å, e.g., about 50 Å to about 100 Å, and depositing the continuous α-Ta layer at a thickness of about 200 Å to about 350 Å, e.g., about 300 Å.

[14] Embodiments of the present invention comprise dual damascene interconnect structures comprising a lower Cu or Cu alloy via in electrical contact with a lower metal feature and connected to an upper Cu or Cu alloy line, wherein the layer of Ta comprises α-Ta, and the dual damascene structure is formed in dielectric layer or layers comprising a dielectric material having a dielectric constant less than about 3.9.

[15] Additional advantages of the present invention will become readily apparent to those skilled in this art from the following detailed description, wherein embodiments of the present invention are described, simply by way of illustration of the best mode contemplated for carrying out the present invention. As will be realized, the present invention is capable of other and different embodiments, and its several details are capable of modifications in various obvious respects, all without departing from the present invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, and not as restrictive.

BRIEF DESCRIPTION OF DRAWINGS

[16] Fig 1 illustrates a typical hysteresis curve during IPVD employing a Ta target and an N_2 flow.

[17] Figs. 2 through 4 illustrate a single damascene embodiment in accordance with the present invention.

[18] Figs. 5 illustrates a dual damascene embodiment in accordance with the present invention.

DESCRIPTION OF THE INVENTION

[19] The present invention addresses and solves various problems attendant upon forming Cu or Cu alloy interconnects, particularly, damascene structures in dielectric layer(s) comprising dielectric material having a dielectric constant (k) less than about 3.9. As employed throughout this application, the symbol Cu is intended to encompass high purity elemental copper as well as Cu-based alloys, such as Cu alloys containing minor amounts of tantalum, indium, tin, zinc, manganese, titanium, magnesium, chromium, titanium, germanium, strontium, platinum, magnesium, aluminum or zirconium.

[20] As design rules are scaled down into the deep submicron range, such as about 0.12 micron and under, electromigration and contact resistance issues associated with Cu interconnects become increasingly significant. Reliability and electromigration issues stem, in part, from the poor adhesion of β-Ta to various low-k dielectric materials and poor adhesion of TaN to Cu and Cu alloys. TaN and β-Ta exhibit high resistivities, thereby adversely impacting circuit speed.

[21] The formation of a composite barrier layer comprising TaN in contact with dielectric material and a layer of α-Ta in contact with the Cu metallization solves adhesion issues generated by the poor adhesion of β-Ta to dielectric material and the poor adhesion of TaN to Cu metallization. It was found that upon depositing Ta on a layer of TaN, the TaN serves as a template for the growth of α-Ta, a low resistivity form of Ta, typically exhibiting a resistivity of about 40 to about 50 μohm-cm vis-à-vis about 170 to about 230 μohm-cm for β-Ta. It was found particularly advantageous to deposit both the composite barrier layers by IPVD, e.g., ionized sputter deposition (ISD). The initial layer of TaN is typically deposited at a thickness of about 25Å to about 150Å, e.g., about 50Å to about 100Å, while the layer of α-Ta is typically deposited at a thickness of about 100 to about 300Å, e.g., about 200Å to about 300Å. The layer of TaN contains nitrogen at a concentration of about 30 to about 65 at.%, e.g., about 40 to about 55 at.%, e.g., about 40% to about 55%.

[22] It should be understood that suitable deposition conditions are dependent upon the particular situation and can be optimized accordingly. It was found suitable, for example, to employ an argon (Ar) flow rate of about 40 to about 60 sccm, e.g., about 45 to about 60 sccm, a N_2 flow rate of about 10 to about 100 sccm, e.g., about 20 to about 70 sccm, a D.C. power of about 1,000 to about 5,000 watts, an RF power of about 1,000 to about 3,000 watts, and a pressure of about 1 to about 45 mTorr, depending upon the particular deposition system and technique. The TaN layer can be deposited for about 3 to about 20 sec., at which point the N_2 flow is turned off and a layer of α-Ta is deposited as for about 10 to about 30 sec.

[23] The present invention comprises a refinement comprising strategically structuring the composite barrier layer to ensure formation of a continuous α-Ta layer, to achieve enhanced electromigration reliability and to improve wafer-to-wafer uniformity. The present invention improves both electromigration performance and wafer-to-wafer uniformity by ensuring the formation of α-Ta layer which is both in the α-form and continuous. The initial TaN layer should, desirably, be deposited as thin as possible for miniaturization and reduced contact resistance. However, it was found that if the initial TaN layer is too thin, the preferred growth orientation for α-Ta in the subsequently deposited Ta layer may not be achieved. It was also

found that the electromigration resistance and wafer-to-wafer uniformity can be improved, and the process margin increased to facilitate fabrication, by structuring the composite barrier layer with a suitable thickness ratio of the α-Ta and graded tantalum nitride layers with respect to the thickness of the initial TaN layers. Embodiments of the present invention include forming the composite barrier layer such that the ratio of the thickness of the α-Ta and graded tantalum nitride layers to the thickness of the initial TaN layer is about 2:1 to about 6:1, such as about 2.5:1 to about 5:1, e.g., about 3:1 to about 3.5:1. Embodiments of the present invention include depositing the initial TaN layer at a thickness no greater than about 100 Å; e.g., about 50 Å to about 100 Å, and ensuring complete cleaning of the Ta target during subsequent deposition to deposit a continuous α-Ta layer at a thickness of about 200 Å to about 350 Å, e.g., about 300 Å. Control of the ratio of the thickness of the α-Ta and graded tantalum nitride layers with respect to the thickness of the initial TaN layer in accordance with the present invention results in Cu interconnect structures having improved electromigration reliability and improved wafer-to-wafer uniformity.

[24] A three barrier layer composite in accordance with an embodiment of the present invention comprises an initial layer of TaN, a graded layer of tantalum nitride on the initial TaN layer, and a layer of α-Ta on the graded tantalum nitride layer. The graded tantalum nitride layer typically has a N_2 content which decreases from proximate the initial TaN layer formed lining the opening to about zero proximate the α-Ta layer, and typically contains α-Ta in an amount which varies from about zero proximate the initial TaN layer to about 100% proximate the α-Ta layer. The initial TaN layer typically has a N_2 content of about 30 to about 65 at.%, while the graded tantalum nitride layer has a N_2 content substantially corresponding to that of the initial TaN layer proximate the initial TaN layer, i.e., about 30 to about 65%, and decreases to about zero proximate the α-Ta layer. The resistivity of the graded tantalum nitride layer depends upon the N_2 content and is typically about 200 to about 900 μohm-cm proximate the initial TaN layer decreasing toward the α-Ta layer. The three barrier layer composite embodiment of the present invention typically has an overall thickness of about 250 Å to about 500 Å.

[25] The present invention stems, in part, from the recognition that the dominant Cu diffusion path for electromigration is along the Cu barrier layer interface at the bottom and sidewalls of a via electrically connecting upper and lower features, and in part from the recognition that the quality of the Cu barrier layer interface depends on the microstructure and crystalline structure of the α-Ta layer which, in turn, depends upon the thickness ratio of the α-Ta and graded tantalum nitride layers to the initial TaN layer.

[26] The three barrier layer composite embodiment of the present invention can be implemented by a strategic ISD deposition technique in which the N_2 flow rate is increased to a level above that employed in conventional practices and yet achieves a desirable stable uniform deposition rate and enables the subsequent formation of the low resistivity α-Ta layer. In Fig. 1 a typical hysteresis curve for ISD is illustrated with the abscissa denoting the N_2 flow rate and the ordinate denoting the target voltage. Conventional practices tend to employ a low N_2 flow rate operating in region I to maintain reactive deposition without poisoning the Ta target with N_2. It should be understood that Ar is also employed during ISD deposition, with N_2 being the reactive species. Region II is not consistent with conventional wisdom in that a small variation in the N_2 flow rate results in a large variation in N_2 target poisoning resulting in an unstable process causing drifts or variations in the deposition rate, such as variations in thickness and composition. The adverse impact of N_2 poisoning on target composition and target surface causing non-uniform deposition results in an uncontrolled process and adversely impacts product-to-product uniformity. Region III is, similarly, not consistent with conventional wisdom due to the high degree of N_2 target poisoning.

[27] It was found that the use of a high N_2 flow rate, in excess of that conventionally employed, i.e., operating in region III, caused a sufficiently high degree of Ta target poisoning such that, upon discontinuing the flow of N_2 subsequent to deposition of the initial TaN layer, deposition conditions can be otherwise maintained to deposit a graded tantalum nitride layer and α-Ta layer thereon, using the N_2-poisoned Ta target containing a surface layer of TaN. By continuing deposition conditions in the absence of flowing N_2, the N_2-poisoned Ta target is actually cleaned of N_2 to form the graded tantalum nitride barrier layer having a decreasing N_2 content and increasing α-Ta content across its thickness proceeding away from the initial TaN barrier layer. As deposition continues, a layer of essentially pure α-Ta is formed on the graded tantalum nitride layer from the cleaned Ta target completing the three composite layer barrier. Experimental results confirmed that electromigration resistance is optimized by forming a three barrier layer composite comprising an initial TaN layer, a graded tantalum nitride layer thereon and an α-Ta layer.

[28] Although the mechanism underpinning the dramatic improvement in electromigration results is not known for certainty, it is believed that the formation of a graded tantalum nitride layer results in optimum adhesion between the α-Ta layer and the initial TaN layer and, by operating in region III, a desirably stable deposition is obtained yielding improved uniformity in composition and thickness. Thus, not only is electromigration resistance enhanced, but product-

to-product uniformity significantly improved. In addition, the advantageous formation of an α-Ta layer results in a significant reduction in contact resistance.

[29] The deposition conditions forming the three barrier layer composite embodiment of the present invention is also dependent on a particular situation and, hence, can be optimized accordingly. For example, it was found suitable to conduct ISD of the three barrier layer composite at an Ar flow rate of about 40 to about 60 sccm, e.g., about 45 to about 60 sccm, an RF power of about 1,000 to about 2,000 watts, and a pressure of about 20 to about 45 mTorr. During initial deposition of the TaN layer, a N_2 flow rate of about 20 to about 100 sccm, e.g., about 35 to about 75 sccm, is employed. After deposition of the initial TaN layer, as after about 5 to about 20 seconds to a thickness of about 50 Å to about 100 Å, the N_2 flow rate is discontinued. The high N_2 flow rate employed during deposition of the initial TaN layer, e.g., about 35 to about 75 sccm, operates in range III (Fig. 3) and poisons the Ta target with N_2 forming a layer of TaN on the Ta target.

[30] After stopping the N_2 flow, ISP deposition continues using the N_2- poisoned TaN target to sequentially form the graded tantalum nitride layer. In accordance with embodiments of the present invention, the initial TaN layer is formed at a sufficient thickness, e.g., about 50 Å to about 100 Å, to ensure functioning as a template for the deposition of α-Ta than β-Ta, e.g., predominately α-Ta vis-à-vis β-Ta . In addition, subsequent deposition using the N_2- poisoned Ta target is continued to ensure formation of a continuous α-Ta layer, as at a thickness of about 200 Å to about 350 Å, e.g., about 300 Å. Embodiments of the present invention include depositing the graded tantalum nitride layer over a period of about 3 to about 15 seconds and to a thickness of about 25 Å to about 100 Å, and depositing the α-Ta layer over a period of about 10 to about 30 seconds.

[31] The graded tantalum nitride layer comprises a mixture of TaN and α-Ta, the N_2 content decreasing and the α-Ta content increasing across the thickness of the graded tantalum nitride layer from proximate the initial TaN layer to proximate the α-Ta layer. Advantageously, the bias power applied during deposition of the initial TaN layer, and/or during deposition of the subsequent graded tantalum nitride and α-Ta layers can be separately optimized. For example, an A.C. bias power of about zero to about 500 watts can be applied during deposition of the TaN layer, and an A.C. bias power of about 200 to about 400 watts can be applied during deposition of the graded tantalum nitride and α-Ta layers.

[32] An embodiment of the present invention comprising a three barrier layer composite in Cu metallization to form a Cu line is schematically illustrated in Figs. 2 through 4, wherein similar

features or elements are denoted by similar reference numerals. Adverting to Fig. 2, a trench 41 is formed in low-k interlayer dielectric 42 overlying layer 40, e.g., an interlayer dielectric. An initial TaN layer 43 is deposited on the side surfaces of low-k interlayer dielectric 42 defining trench 41. Initial TaN layer 43 is deposited by ISD at a sufficiently high N_2 flow rate, e.g., about 35 to about 75 sccm, to poison the Ta target with N_2, forming a surface layer of TaN having a suitable thickness to ensure growth of the subsequently deposited Ta layer in a preferred orientation to attain the α-Ta structure, e.g., as at a thickness of about 50Å to about 100Å. During deposition of initial TaN layer 43, a bias power up to about 500 watts can be applied to the substrate.

[33] After deposition of the initial TaN layer 43, the N_2 flow is shut off and ISD continues utilizing the N_2-poisoned Ta target. During such continued deposition using the N_2-poisoned Ta target without the flow of N_2, a graded tantalum nitride 44 is deposited. Such continued deposition is continued to ensure that the N_2-poisoned Ta target is completely cleaned, i.e., the surface layer of TaN is completely removed, and an essentially pure continuous α-Ta layer 45, having a thickness of about 200 Å to about 350 Å, is formed on graded tantalum nitride layer 44. Typically, the initial TaN layer 43 has a N_2 content which decreases from about 30 to about 65 at.% and the graded tantalum nitride layer 44 has a N_2 content of about 30 to about 65 at.% proximate the initial TaN layer 43 decreasing to zero proximate the α-Ta layer 45, while the concentration of α-Ta within the graded tantalum nitride 44 layer is about zero proximate the initial TaN 43 layer increasing to about 100% proximate the α-Ta layer 45. The resistivity of the graded tantalum nitride layer 44 decreases from a value between about 200 to about 900 μohm-cm at the initial TaN layer 43 toward the α-Ta layer 45. The α-Ta layer 45 exhibits a resistivity considerable lower than that of the conventionally deposited β-Ta layer. The resistivity of α-Ta layer 45 typically ranges from about 40 to about 50 μohm-cm, while the resistivity of a conventionally deposited β-Ta layer is typically about 170 to about 230 μohm-cm.

[34] Fig. 3 represents an expanded view of region A of Fig. 2 showing the relatively high and substantially constant N_2 concentration of the initial TaN layer 43, and the decreasing N_2 concentration of the graded tantalum nitride (TaN_x) layer 44. Also depicted are the Cu metallization and α-Ta layer 45.

[35] Subsequently, a seedlayer 60 can be deposited on continuous α-Ta layer 45, and the trench 41 is filled with Cu, as by electroless deposition or electroplating. CMP is then conducted to planarize the upper surface resulting in the structure schematically illustrated in Fig. 4 containing Cu line 61. The three barrier layer composite advantageously provides enhanced

electromigration resistance, believed to be due in part to the improved Cu barrier layer interface by ensuring the formation of a high quality, continuous α-Ta layer 45.

[36] The embodiment illustrated in Figs. 2 through 4 relates to a single damascene structure. However, it should be understood that the present invention is also applicable to dual damascene structures. For example, a dual damascene structure formed with the three barrier layer composite embodiment of the present invention is schematically illustrated in Fig. 5, wherein a lower metal feature 81, e.g., a Cu line, is formed in an underlying dielectric layer 80, e.g., a dielectric layer containing a low-k dielectric material. Also illustrated in Fig. 5 is a capping layer 82, such as silicon nitride or silicon carbide, dielectric layer 83 and dielectric layer 84 separated by middle etch stop layer 85, such as silicon nitride or silicon carbide. Dielectric layers 83 and 84 can comprise a low-k dielectric material. A dual damascene opening is formed by any conventional technique, such as a via first-trench last or trench first-via last technique. An initial layer of TaN 85 is deposited by ISD using a N_2 flow rate sufficient to poison the Ta target. After depositing initial TaN layer 85, the N_2 flow is discontinued and ISD continued using the N_2-poisoned Ta target to sequentially deposit graded tantalum nitride layer 86 and a continuous, essentially pure layer of α-Ta 87. A seedlayer 88 can then be deposited followed by Cu deposition, e.g., electroplating or electroless deposition, and CMP is then conducted to form Cu line 89A connected to Cu via 89B which is in electrical contact with underlying metal feature 81. A capping layer 801, such as silicon nitride or silicon carbide, is then deposited to complete the interconnect structure illustrated in Fig. 5. In accordance with embodiments of the present invention, the initial TaN layer 85 is formed at a sufficient thickness, e.g., about 50 Å to about 100 Å, to ensure subsequent deposition of α-Ta. In addition, the ratio of the thickness of the combined α-Ta layer 87 and graded tantalum nitride layer 86 to the thickness of the initial TaN layer 85 is controlled to about 2.5:1 to about 5:1, e.g., about 3:1 to about 3.5:1, to ensure formation of a high quality Cu |α-Ta interface for improved electromigration performance and improved wafer-to-wafer uniformity.

[37] In implementing various damascene techniques in accordance with embodiments of the present invention, Cu can be deposited by electroless deposition or electroplating using a seed layer. Typical seed layers include Cu alloys containing magnesium, aluminum, zinc, zirconium, tin, nickel, palladium, silver or gold in a suitable amount, e.g., about 0.3 to about 12 at.%. CMP is then performed such that the upper surface of the inlaid Cu is substantially coplanar with the upper surface of the interlayer dielectric.

[38] In accordance with embodiments of the present invention, the damascene opening can also be filled with Cu by PVD at a temperature of about 50°C to about 150°C or by CVD at a

temperature under about 200°C. In various embodiments of the present invention, conventional substrates and interlayer dielectrics, can be employed. For example, the substrate can be doped monocrystalline silicon or gallium-arsenic. The interlayer dielectric employed in the present invention can comprise any dielectric material conventionally employed in the manufacture of semiconductor devices. For example, dielectric materials such as silicon dioxide, phosphorous-doped silicate-glass (PSG), boron-and phosphorus doped silicate glass (BPSG), and silicon dioxide derived from tetraethylorthosilicate (TEOS) or saline by PECVD can be employed. The openings formed in dielectric layers are effected by conventional photolithographic and etching techniques.

[39] Advantageously, dielectric materials for use as interlayer dielectrics in accordance with embodiments of the present invention can comprise dielectric materials with lower values of permitivity and those mentioned above, in order to reduce interconnect capacitance. The expression "low-k" material has evolved characterized materials with a dielectric constant less than about 3.9, e.g., about 3.5 or less. The value of a dielectric constant expressed herein is based upon the value of (1) for a vacuum.

[40] A wide variety of low-k materials can be employed in accordance with embodiments of the present invention, both organic and inorganic. Suitable organic materials include various polyimides and BCB. Other suitable low-k dielectrics include poly(arylene)ethers, poly(arylene)ether azoles, parylene-N, polyimides, polynapthalene-N, polyphenylquinoxalines (PPQ), polyphenyleneoxide, polyethylene and polypropylene. Other low-k materials suitable for use in embodiments of the present invention include FO_x^{TM} (HSQ-based), XLK™ (HSQ-based), and porous SILK™, an aromatic hydrocarbon polymer (each available from Dow Chemical Co., Midland, MI); Coral™, a carbon-doped silicon oxide (available from Novellus Systems, San Jose, CA), silicon-carbon-oxygen-hydrogen (SiCOH) organic dielectrics, Black-Diamond™ dielectrics, Flare ™, an organic polymer, HOSP™, a hybrid sioloxane-organic polymer, and Nanoglass™, a nanoporous silica (each available from Honeywell Electronic Materials) and halogen-doped (e.g., fluorine-doped) silicon dioxide derived from tetraethyl orthosilicate (TEOS) and fluorine-doped silicate glass (FSG).

[41] The present invention enables the manufacture of semiconductor devices having Cu interconnects with improved electromigration resistance, enhanced reliability, reduced contact resistance and improved wafer-to-wafer uniformity. Forming an initial TaN layer of sufficient thickness and continuing post TaN layer deposition for a sufficient period of time enables deposition of a continuous, essentially pure α-Ta having a significantly reduced resistivity vis-à-vis β-Ta typically formed using conventional deposition techniques. Electromigration resistance

and wafer-to-wafer uniformity is improved by forming a high quality Cu barrier layer interface by controlling the relative thickness of the combined α-Ta and graded tantalum nitride layers with respect to the thickness of the initial TaN layer.

[42] The present invention enjoys industrial applicability in the formation of various types of inlaid Cu metallization interconnection patterns. The present invention is particularly applicable to manufacturing semiconductor devices having submicron features and high aspect ratio openings.

[43] In the previous description, numerous specific details are set forth, such as specific materials, structures, chemicals, processes, etc., to provide a better understanding of the present invention. However, the present invention can be practiced without resorting to the details specifically set forth. In other instances, well known processing and materials have not been described in detail in order not to unnecessarily obscure the present invention.

[44] Only the preferred embodiment of the present invention and but a few examples of its versatility are shown and described in the present invention. It is to be understood that the present invention is capable of use in various other combinations and environments and is capable of changes or modifications within the scope of the inventive concept as expressed herein.